Experiments with a QRO 500kHz Class E Power Amplifier

Andy Talbot G4JNT Jan 2011

Having read plenty of discussion on the LF Reflector from people who have built used Class E switch mode amplifiers, I thought I'd see what could be done in the way of a low cost high power unit for 503kHz. A target power output of 500 Watts running from a 50V supply was decided upon as an aiming point

References [1] and [2] provided all the design details, and I generated a version of Alan's design spreadsheet [3] that added a series L / shunt C matching network to the output to raise Rload up to 50 Ohms. The series L is absorbed into either the tank circuit L or C values.

The junk box gave up several IRFP462 FETs – these are rated at 500V, 170 Watts dissipation and Rds on of 0.4 ohms – a bit high but would have to do for now. For driving the FETs I had a few ICL7667 devices, together with a host of bits and pieces recovered from SMPSUs over the years. Also, plenty of 2.5mm plastic covered Litz wire to wind the tank coil. Capacitors would have to be rated at several hundred volts, and not having many suitable ones of different values, I ordered a batch of 1kV disk ceramics of values from 470pF to 4.7nF, in order to be able to make up different values for tuning and to use several in parallel to share current.

Discussion on the LF reflector suggested two devices in parallel would be needed, at least, for this sort of power, and one comment suggested the ICL7667 was only just up to the task. The circuit in Figure 1 was put together, with input circuitry consisting of a bandpass filter followed by a line receiver to get a close-to-50% duty cycle square wave from a low level input. Since the ICL7667 contains two identical drivers, both were used together. One for each of the parallel FETs to reduce the loading due to the FET's 2000pF of input capacitance amplified by Miller feedback.

The design was built up using parallel disc-Cs to get as close as possible to the calculated values from the spreadsheet, and the unit was powered initially with a 12V supply to the PA in order to view the switching waveforms safely. The result was appalling – terrible – useless! The waveforms looked nothing at all like they should do in [1] and [2] – clearly the component values were very-very wrong.

Using an LC meter to measure the capacitors showed what had happened. These capacitors had the most appalling temperature coefficient I have ever seen! One of the 10nF capacitors would occasionally measure about 10nF at room temperature but as soon as it was warmed, or even when I blew on it, the value shifted dramatically. Applying a soldering iron to one of its leads, dropped the 10nF down to 5.3nF. All were consigned to the waste bin. Should have read the specs – the fine print does say they have a temperature coefficient in the -20 to +80% region over 0 – 60 degrees.

Fortunately, the junk box also threw up two 22nF 1000V poly-propylene capacitors – which were close to two of the wanted values, and a large number of 3.3nF 1700V ones. (These were left over from my very first attempts on 73kHz back in 1997 – having been used to resonate a loop antenna before abandoning that for the more efficient vertical). The quantisation of the resulting capacitance value using these in parallel, with 3.3nF increments, would possibly be a bit coarse, but would do to start with. The first breadboard using these can be seen in *Photo 1*, and with a bit of trimming the right shape of waveform began to appear.

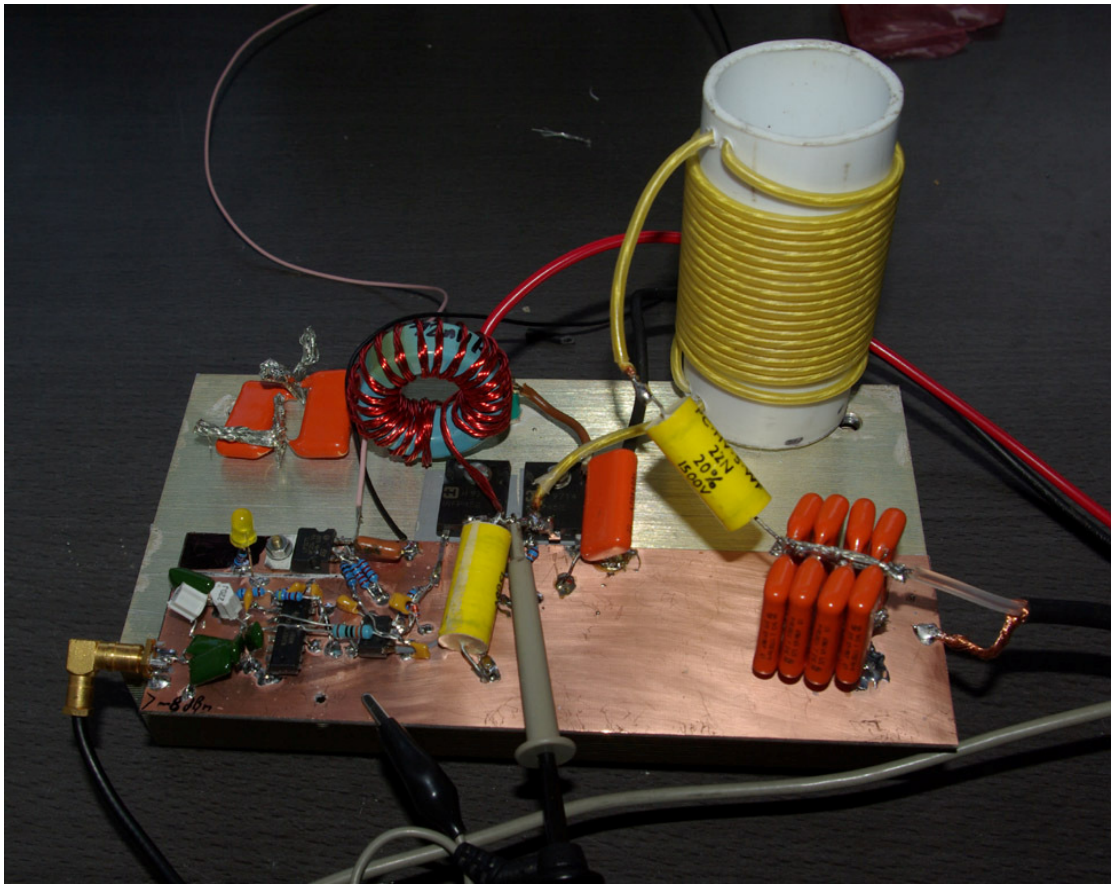

Photo 1 - First Breadboard Version

Using the high current PSU, and winding the voltage up slowly did begin to give a decent amount of power, but at 40V supply, when it was delivering just short of close to 300 Watts I could feel a fair bit of heat coming off the board. The heatsink was cool, but C1, the yellow cap in shunt with the FETs was running rather warm, and the DC feed choke was quite hot.

The two 22nF caps were replaced with parallel combinations of the 3.3nF ones and the number of these in each position juggled to give first the correct switching waveform then at varying supply voltages aiming for a decent power output level at 50 Volts. Several combinations were found that gave lower output power, but the values finally ended up as those in *Figure 1*.

After several minutes of test at full power, the original 50uH DC feed choke, consisting of 25 turns of home made Litz wire on an iron dust toroid recovered from an SMPSU was running very hot – well above 100C so had to be replaced. A larger toroid was found, already wound with more turns of thicker Litz and measured 100uH. When the DC feed was replaced with this, it ran cool with a marginally higher output power. At full power, the switching waveform is as shown in *Photo 2*. Both traces are 50V / division. The final breadboard can be seen in *Photo 3*.

Results

Vdd (Volts)	Id (Amps)	Power Input	Power Out	Efficiency
31.3	6.5	202	163	81%
37.4	7.6	286	230	81%
43.6	8.8	387	311	80%
50	10.1	507	400	79%

It can be seen that there is something like 8V across the device during its on time, and this is no doubt contributing to the power loss and reduced efficiency. Also, the edges of the FET drive waveform are not ideal – although whether this contributes to a slower device turn on is unknown. Sharper edges would be nicer.

Conclusions

Efficiency is not as high as can be obtained from Class E PA stages, - suggested values in excess of 90% have been claimed - but this can be laid down to my using old devices with a high on-resistance.

The target of 500 Watts wasn't achieved, although it may be possible to get there by raising the supply voltage to 60V or more. The peak voltage across the devices with a 50V Vdd is 190V, well short of their maximum 500V, so there is plenty of scope for increasing Vcc. The heatsink runs cool when the fan is running, so again a higher supply voltage may be quite safe.

The component values proved remarkably tolerant – starting off with those generated by the design spreadsheet, then adjusting under test to optimise the switching waveform while using a low supply voltage.

References

[1] http://www.alan.melia.btinternet.co.uk/classepa.htm

[2] http://www.cs.berkeley.edu/~culler/AIIT/papers/radio/Sokal%20AACD5-poweramps.pdf

[3] http://www.g4jnt.com/DownLoad/classe_match.xls

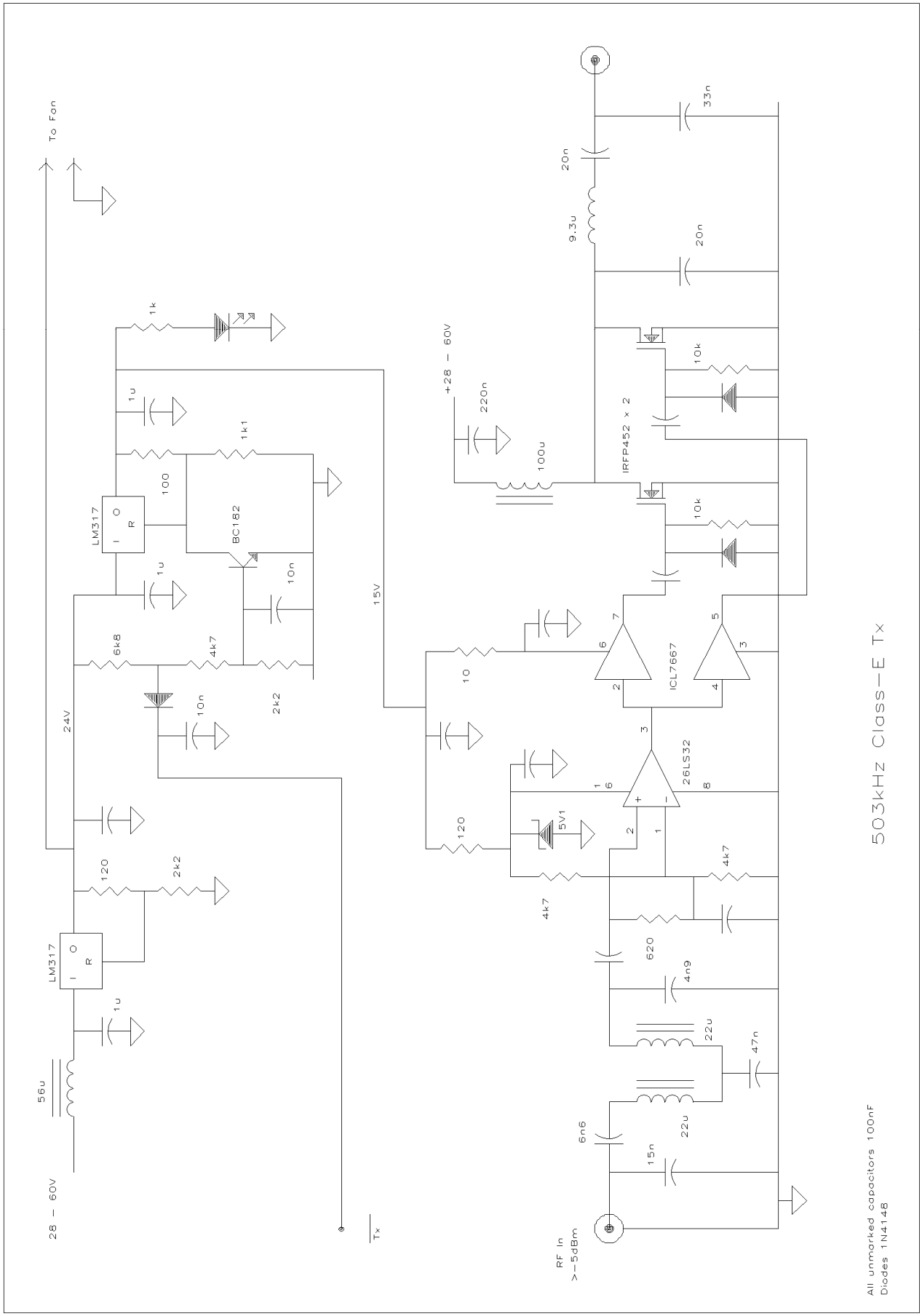

Figure 1 - Circuit Diagram

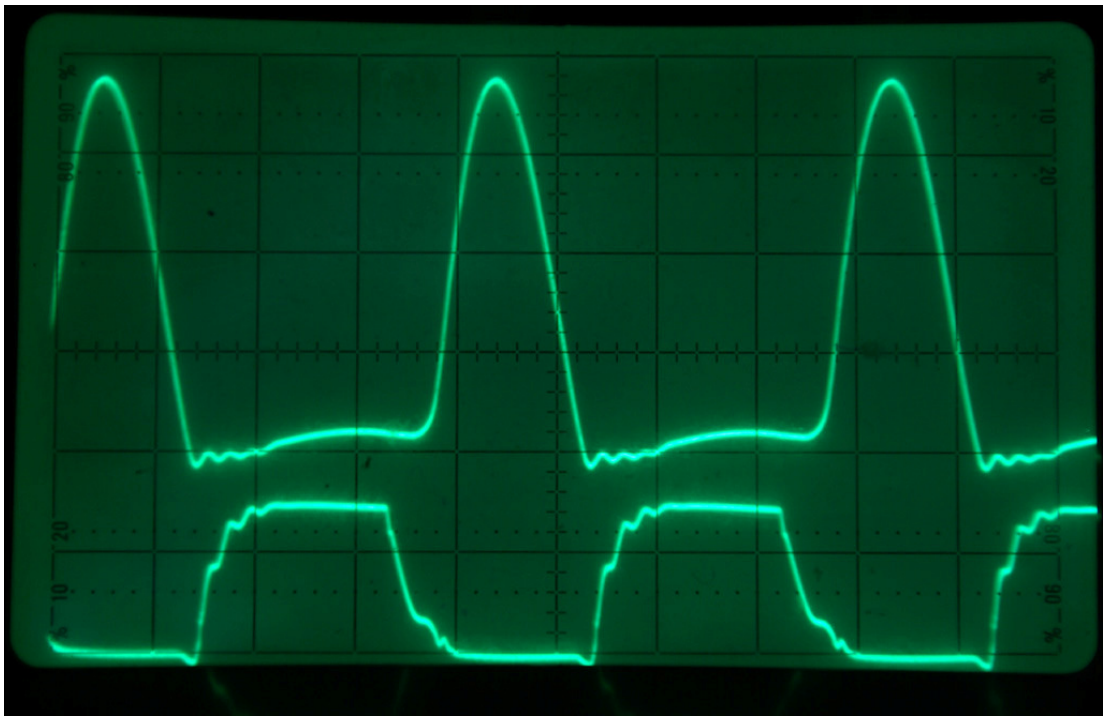

Photo 2 - Switching Waveforms. Top - Vdrain 50V/div. Bottom - FET Drive 10V/div

	Zo	50							
Design Frequency =		503000	Hz	w =2*pi*F	3160449.6				
VRBcev or Vddmax		500	volts						
Select a value for Vcc (Vdd)		50	volts	Vcc (Vdd) must be <		146	volts		
	Vce(sat)	8	volts	Maybe Ic(pk)*rdss is the best guess for a FET					
	Pout	410	watts						
	Ql	7.5	must be greater than 1.8						
----------						Peak voltage Vcc(pk)		157.60	volts
Unmatched —	Series L2	5.89	uH	Resonance	L2/C2	Peak current Ic(pk)		24.95	amp
	Series C2	20.30	nF	460263.83	Hz				
	Rload	2.48	ohms						
Device shunt C1		25.77	nF						
Matching C Absorbed into L2		9.3	uH	C2 =	20.30	nF			
or absorbed into C2		5.89	uH	C2 =	67.0	nF			
Output shunt C3		27.7	nF						
Bias choke min		23.6	uH		Xc2	15.6	j ohms		
					Output L Matching				
Output at reduced Vcc					Xl ser	10.9	j ohms		
New Vcc		31	V		Xc ‖	11.4	j ohms		
Pout		157.6	Watts		Additional Series L	3.4	uH		
					residual Xc2	4.7			

Design Spreadsheet showing the approximate starting values

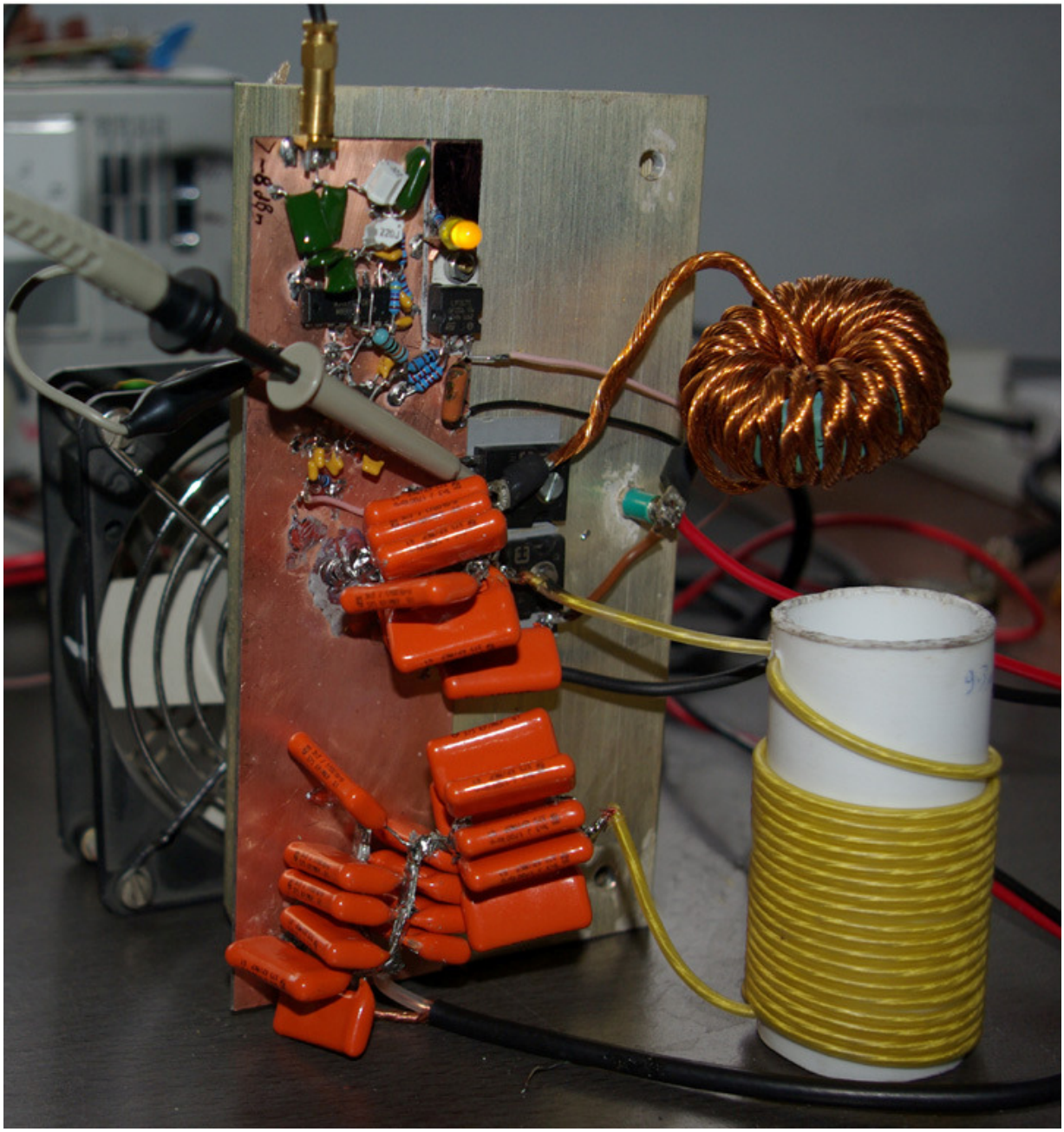

Photo 3 - The Final Breadboard