Direct Upconverting Beacon Driver Source

As Used on GB3SCS

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Background

The Bell Hill family of microwave beacons, GB3SC#, operating on the 2.3 to 24GHz amateur bands have been gradually developed and enhanced over a period of more than 25 years. [1] The earliest ones started out as simple free running crystal oscillator / multiplier designs using on-off Morse keying for their ident. Over the years these beacons progressed through frequency locking to a master reference locked to GPS and then adding multi-frequency WSJT modes to the keying sequence. At each upgrade, to make use of existing hardware as much as possible, the 3.4 to 24GHz beacons all adopted the 'reverse DDS' locking technique detailed at [2].

GB3SCS on 2.3GHz was the exception. When the original beacon failed the RF multiplier chain that was in poor shape was abandoned and a new driver designed. This was based on an AD9852 DDS running from a clock derived from the master reference. The DDS output was at close to 2.4MHz which was subsequently multiplied up in a PLL multiplier [3]. Surplus hardware was used for the PLL module which had a relatively wide loop bandwidth for this application. The DDS output after multiplication by nearly 1000 times had a fair number of discrete spurii and poor phase noise, to the extent it could be heard by several local station who raised a couple of complaints.

When the beacon complex developed a fault that required master hardware to be replaced, the opportunity was taken to rebuild the driver for GB3SCS using a new technique providing more flexibility for upgrading.

Direct Quadrature Upconversion

Several breadboard test modules had been developed and characterised over the years for direct upconversion from a baseband signal delivered as an I/Q pair, with the RF coming from a fixed frequency source. An overall description of several upconverter chips and other solutions can be found at [4] and [5]. By generating the baseband waveform using negative and positive frequencies - possible because they are delivered as an I/Q pair - any image or carrier leakage components will sit on top of the wanted output. Provided these unwanted components are more than -15dBc they will not degrade the wanted signal, and being co-channel will not interfere with adjacent frequency usage.

For GB3SCS the ADF8346 quadrature upconverter chip looked suitable for the mixer as it covers the range 800 – 2500MHz, so the original breadboard module used for those initial tests at [4] was extracted from storage and pressed into service. The circuit of this is shown in Figure 1. Level shifting is needed to go from the unipolar higher voltage output from the baseband source to the differential voltage drive that the upconverter chip requires. To simplify this on the hardware used here, AC coupling was adopted. This means that for a small frequency range, either side of DC, there is a 'hole' in the middle of the upconverted spectrum perhaps a few Hertz wide. The width of this hole depends on the time constant of the AC coupling components used; on this breadboard they were of the order of 130ms, leading to a single pole high pass response at 1.2Hz, with a resulting hole 2.4Hz wide. It would be necessary to choose an I/Q drive waveform that had no components at zero frequency, ie. there must not be any tone energy exactly mid-band.

This can be guaranteed when modes with only a few wide spaced tones are to be generated, such as for the JT4G modulation used on the higher frequency Bell Hill beacons. JT4G was used on upconverter tests in the past as this mode uses just four frequencies spaced 315Hz apart. By placing the middle two tones

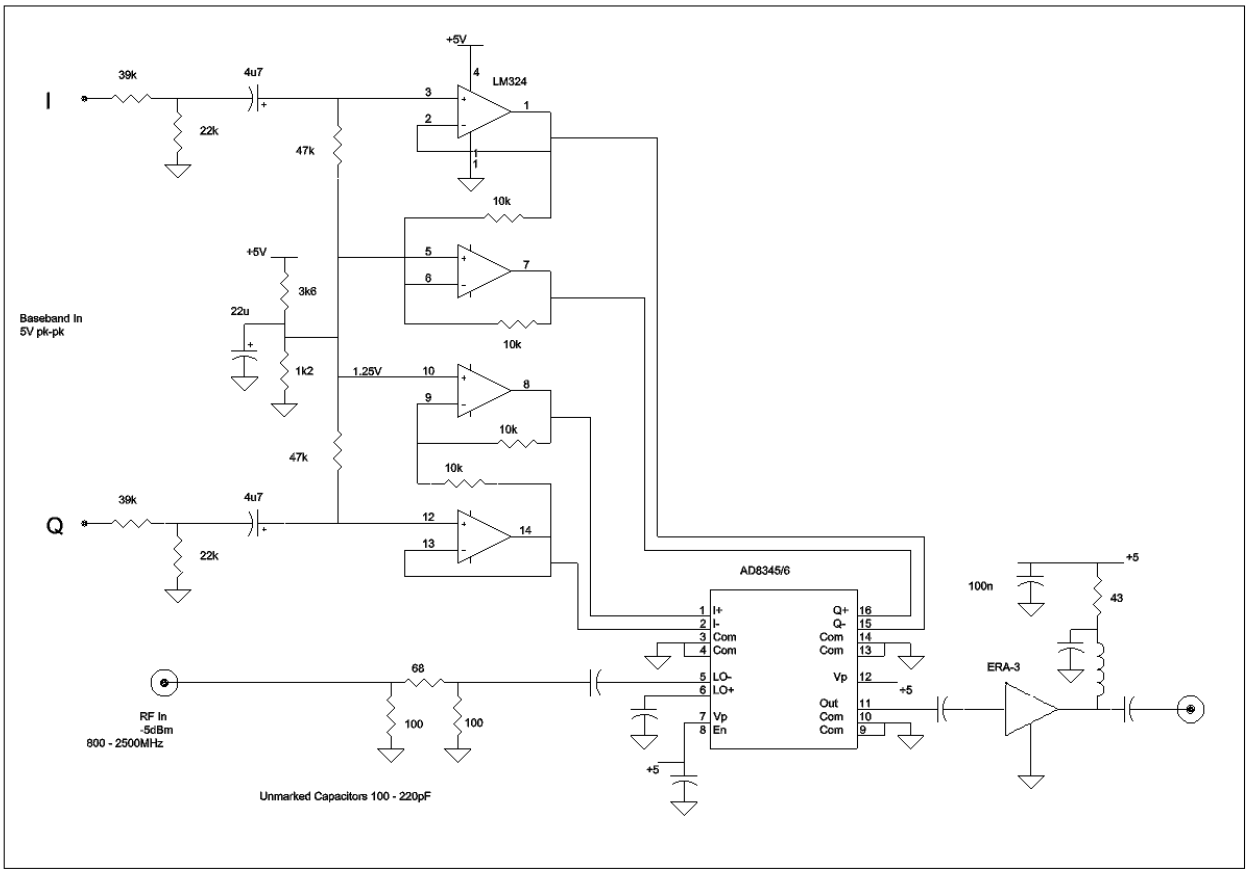

Figure 1 ADF8446 Quadrature upconverter with single ended to differential drive circuitry

either side of the centre hole, the minimum frequency of the baseband component is 315Hz/2 or 175.5Hz; well away from the centre hole. For GB3SCS it was hoped to be able to use a different modulation, Q65-D, with 65 tones just 13.33Hz apart. Tests would have to be made to see if the AC coupling degraded the waveform in any way.

Carrier leakage through the upconverter device was measured at around -30dBc, and the unwanted image around -40dBc. As these signals fall within the same passband as the wanted signal, that cannot be considered to 'out of band'. At this level they are significantly below the -15dBc that would pose no problem or degradation in the decoder. In practice these are below the noise level and thus unobserved for most weak signal reception.

Generating the Quadrature Baseband Waveform

A variable frequency source needs to be defined that can generate arbitrary frequency tones in the range -900z through zero (DC) to +900Hz. This spread will cover all the MFSK WSJT modes likely to be used in the future. Two baseband DDS ideas have been developed. The first used a 16F870 PIC processor which had plenty of I/O lines. 16 of these were used to drive two identical 8-bit R-2R ladders. The PIC firmware was controlled via a timer driven interrupt at a sampling rate in the region of 48kHz. A Numerically Controlled Oscillator in conjunction with an 8 bit sine lookup table allowed a low frequency DDS to be constructed, outputting a quadrature waveform.

Initially several audio tones were pre-programmed into the processor memory with the appropriate one selected using additional pins on the processor. This allowed a separate modulation controller to select which one of a small set of tones to generate, using the parallel bus to communicate with the DDS. Subsequently a pseudo-SPI interface was incorporated into the Audio DDS firmware to give greater flexibility and give full 24 bit control of the tone output frequency, allowing any value to be set within its full tuning range. This was done using 'bit-banging', reading the three incoming SPI signals in-between the sampling rate interrupts.

Provided the incoming SPI signals (clock, data and strobe) transition slow enough to ride-out the sample / interrupt timing, the SPI functions seamlessly. For the controller generating the modulation, this is no different in concept to generating the SPI signals to control a 'real' RF DDS – except it has to be slower. In practice just a few lines of PIC code needed to be changed in a controller that originally generated WSJT MFSK modes directly at RF from an AD9851 DDS chip.

An SPI clock pulse interval of 200µs was adopted in the WSJT mode generator to allow for any future baseband DDS hardware running at a slower sampling rate. This pulse interval should allow unimpeded pseudo-SPI operation with a DDS interrupt firing at 10kHz or faster for its sampling. A PIC device with integral SPI hardware would allow faster operation at the speeds in use here, but it was felt the increased complexity of adopting a processor chip with the necessary peripheral interface wasn't worth it.

Improved Baseband DDS

The R-2R ladder DDS was a bit cumbersome and resistor tolerances in the ladder, together with slight output pin voltage level variations, meant the generated waveform was not as clean as it could be. Harmonics, and some of the complex, difficult to determine, products that are seen in DDS sources were a bit higher than ideal. So a new design of quadrature DDS was developed using a two channel D/A converter instead of the discrete R-2R ladder. A 16F628A PIC communicates with this via another faster SPI interface. As this is also generated by bit-banging, some processor timing overhead is needed to send the 32 bits per sample needed for this D/A converter chip. A lower sampling rate of 16384Hz was therefore chosen. With baseband audio being generated at below 1kHz, this sampling rate is still way above any Nyquist limit, and allows simple anti-alias filtering in a pair of Opamp 2-pole filters. Figure 2 shows the circuit diagram of this I/Q baseband DDS source. Although two SPI interfaces are in use, one reading incoming frequency data and one writing to the D/A, both implemented using bit-banging, a processor oscillator of 19.6608MHz still gives plenty of timing margin. This baseband DDS was used for the new direct upconversion beacon hardware.

One possibility being looked at for the future, although not yet developed into having SPI control, is to use the vastly enhanced 16F1827 PIC device as a single-chip baseband DDS source. This has dual Pulse Width Modulation outputs which can be used to replace the external 2-channel D/A converter. Its architecture allows a 10 bit sine lookup to make optimum use of the PWM generators, a 1024 point sine table, as well as a faster NCO giving several dB improvement in signal fidelity. It also has hardware SPI interfacing, although whether this can operate simultaneously with two PWM peripherals remains to be seen.

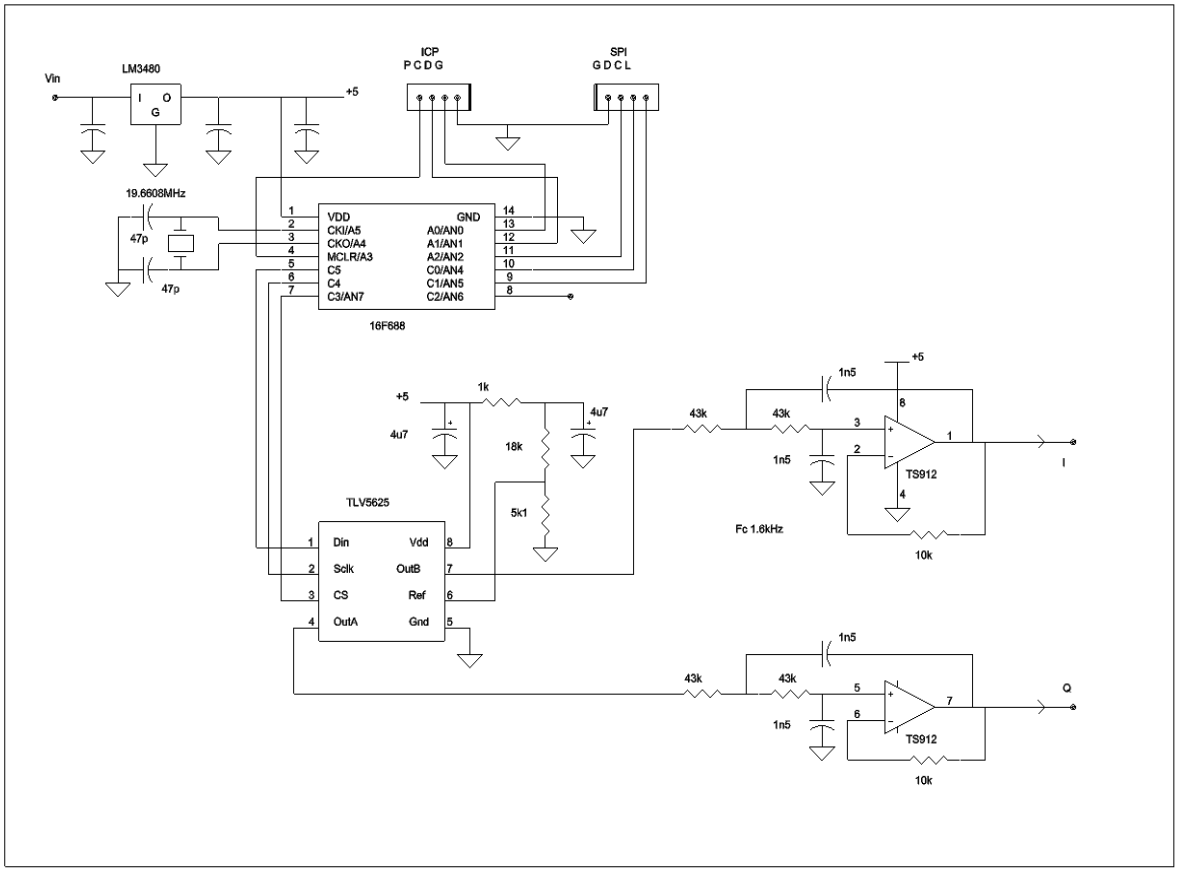

Figure 2 Baseband DDS generating I/Q frequencies in the range -1000 to + 1000Hz

RF Source

The complaints received of spurious signals on the original beacon were believed to be related mainly to the large number of closely spaced discrete spurii that were generated by the multiplied-up DDS. Some were in the -40 dBc region and spaced a few tens of kHz way from the wanted signal, very audible to local stations. As typical amateur transverters used on 2.3GHz are of a design that uses an AD4153 PLL local oscillator, it was felt that an RF source with a similar phase noise performance could be allowed, but discrete spurii kept well down.

Since one was to hand, an off the shelf ADF4351 Fractional-N synthesizer module designed by SV1AFN was used to generate the RF. This is believed to be broadly comparable in phase noise performance with the synthesizer used in the popular transverters. If, subsequently, its phase noise is still considered excessive the RF source can be replaced with a better design without having to change the rest of the beacon driver. For extreme phase noise performance a crystal / multiplier could be used to drive the AD8346 upconverter.

Using a custom utility [6] that allowed registers to be changed on the fly, settings were selected in the ADF4351 that appeared to give the best phase noise at frequency spacings where most interference would be seen. Figures 3 shows the measured phase noise spectrum.

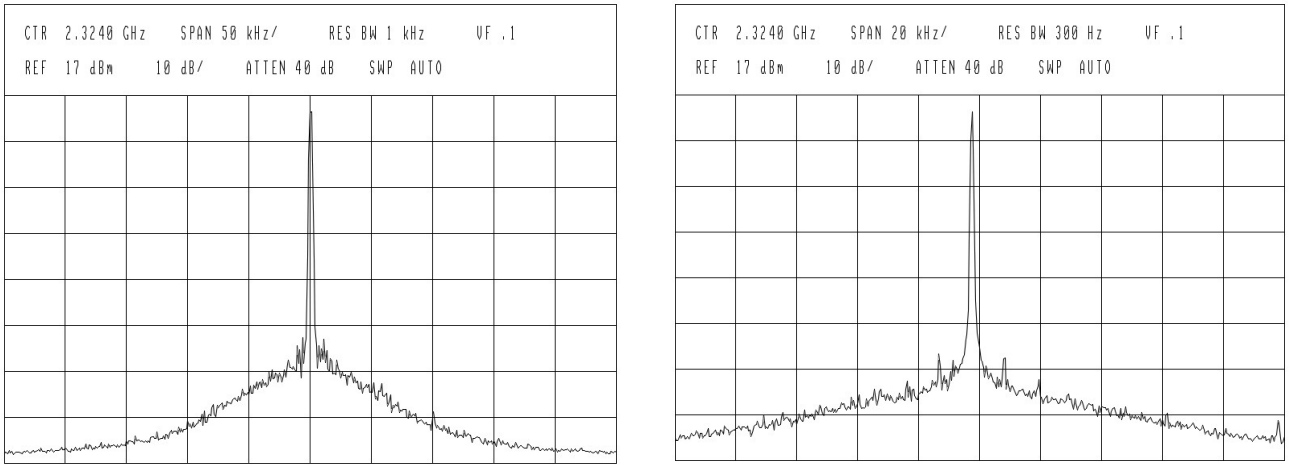

Figure 3 Phase noise of ADF4351 Source at 2.3GHz using a Leo-Bodnar GPSDO as a 10MHz reference input.

Hardware Integration

The SV1AFN synthesizer module, along with a PIC to set its registers at turn on and a 3.3V regulator were installed in a tinplate box. The beacon hardware has a GPSDO to supply the 10MHz reference signal and there is a delay of a couple of seconds after powering up before RF appears. If the ADF4351 has its registers set before the reference signal appears, its internal VCO calibration process fails and the PLL will never lock up. The PIC controller was modified to add a 10 second turn on delay before sending the register contents to allow for the 10MHz to stabilise

The AD8343 breadboard module built several years ago was designed for sound level audio input, ie 1V peak-peak AC coupled. The baseband DDS delivers a 2.5V pk-pk waveform, so to match the existing upconverter's requirements this was simply potted-down to get the correct drive level. This upconverter module, which includes an ERA-3 RF output amplifier, was already built into a tinplate box along with the opamp driver for the baseband single-ended to differential drive conversion. Input level for this chip is specified as -15dBm, so an attenuator was inserted to get optimum RF drive from the synthesizer. The two low frequency modules, the baseband DDS and the modulation / keyer were used without any extra housing. All four modules were mounted on a single baseplate that could be dropped into the old beacon chassis where the power amplifier, on-off keying circuitry and power supply switching remained unchanged. The keyer PIC firmware was modified to generate an inverted CW output so it could drive the PIN diode RF switch directly.

Frequency Planning

Two frequency sources, RF and baseband, are mixed to generate the final output. So there is scope to optimise their relative settings by tweaking the baseband tone set and the exact RF generated by the synthesizer. GB3SCS has to generate the transmitted carrier and the on/off CW on 2320.905MHz exactly. By convention, the later WSJT modes are specified such that the lowest tone, tone-zero, is defined as the reference. IARU recommendations for MGM modes on beacons suggest this base tone is placed on the nominal carrier. The Q65-D modulation intended has 65 tones, labelled T0 to T64, spaced 13.33Hz apart, giving a total spread of 853.Hz.

To avoid the need for a response at DC the centre of the spread, where the AC coupling hole sits, was initially placed between T31 and T32, at 420Hz above the reference. The resulting baseband tone frequency would then range from -420 to +433.3Hz, with the lowest frequency component then becoming 6.7Hz, generated by either T31 or T32.

The RF source appears at the centre of the spread at zero frequency I/Q input, but the lowest tone has to correspond to the reference of 2320.905MHz. This means the synthesizer would have to generate its RF at 2320.905420MHz. The ADF4351 does not have the large fractional-N denominator range of other Fract-N engines, it can only take on values up to 4096, so generating .90542 would take a bit of ingenuity. A search facility was added to the customised ADF4351 control software that tested all ratios of F and D settings to get the nearest to the wanted value possible. The exact frequency is then recalculated and any correction needed can be made by slightly tweaking the baseband DDS setting. A set of values that generated a frequency 0.95Hz low was found with a Fract-N synthesizer F/D of 269/2971 x 10MHz = .90541905, so the DDS was adjusted to start with Tone0 at -419.05Hz.

This software for calculating the register values then optionally programming the registers of the ADF4351 via a serial link and PIC interface is included in the software download at [6].

Glitches

After integration and testing of the whole beacon, a monitor on the RF power output showed that there were several significant drops in output while the Q65-D sequence was being transmitted. In

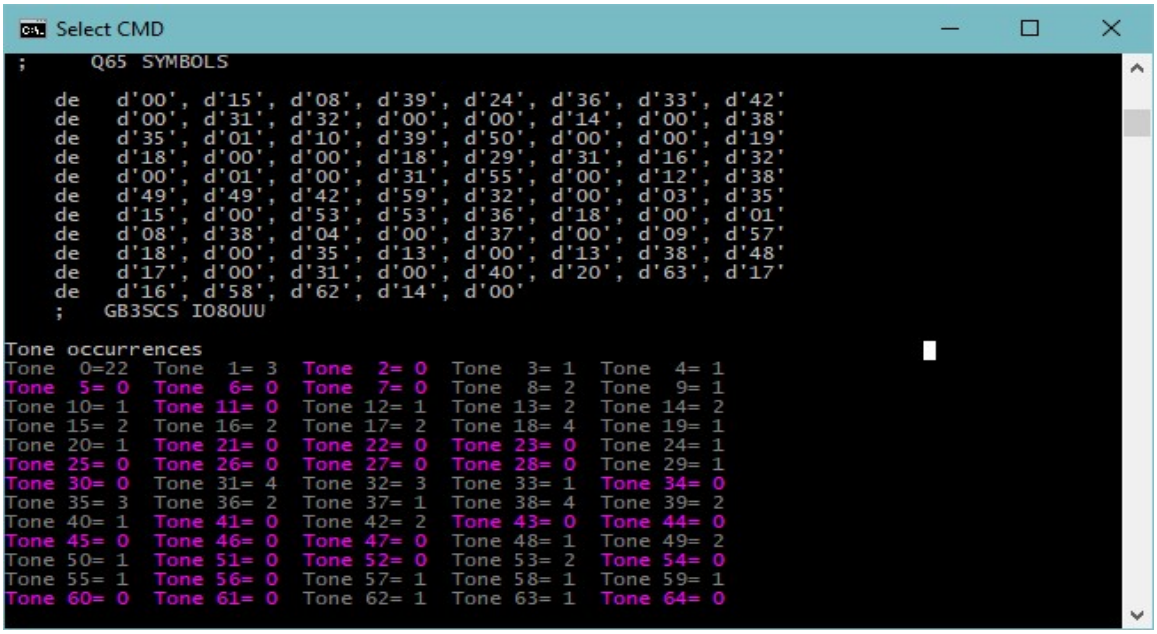

Figure 4 Q65-D Tones and number of occurrences for this beacon message

total there were seven of these and the worst appeared give about 1.5 to 2dB drop. Looking at the set of tone numbers for the programmed message shown in Figure 4, as well as the exact timings when each drop occurred, it could be seen that the drops in power corresponded to T31 or T32 being sent. Clearly the 6.7Hz guard band was insufficient for the AC coupling used in the hardware.

A better frequency offset is possible if the message centre hole can be placed on a tone number that is not used in this particular message sequence. This ensures the minimum frequency presented to the upconverter is at least 13Hz. Examining the tone set for a valid non-used tone is made easier by modifying the utility used to generate the PIC code for the tones. A count of the occurrences of each tone number is shown, with all those not used for that particular message highlighted. For this message, T30 is missing which, serendipitously, just happens to be at 400Hz. Any other message will have to be treated on its own merits for the most suitable placing of the centre frequency.

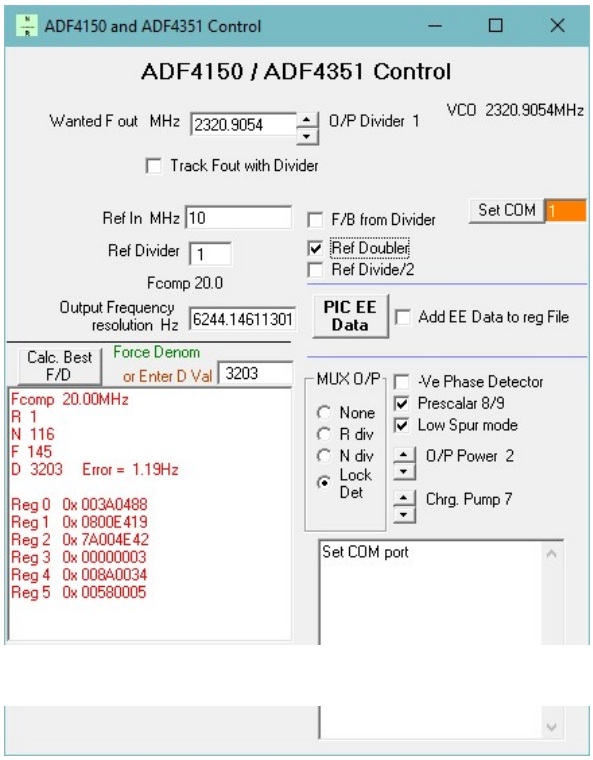

Figure 5 ADF4351 Register set finally adopted for best overall phase noise at 2.3GHz

Another go at reoptimizing phase noise by reprogramming the synthesizer suggested that a marginal improvement was possible by using the reference doubler. The comparison frequency for the PLL phase detector now becomes 20MHz which is even more constraining when trying to hit some arbitrary frequency. The final register set adopted was N + F/D = 116 + 145 / 3203 which at 20MHz F_{COMP} generates a frequency of 2320.9054012 MHz (1.2Hz high). The Baseband DDS setting was adjusted for Tone0 = -401.2Hz to give a 2320.905000 output on carrier and a Tone zero frequency that is at least as accurate as the GPSDO allows. The final register set is shown in Figure 5.

Conclusions and Future Enhancements

Observation of the beacon output power as the tone sequence is transmitted shows a change of perhaps 0.2 to 0.3dB due to the AC coupling and the DDS anti-alias filtering. These variations are less than the older SSB filters in traditional analogue radios can introduce as passband ripple, and certainly less than selective fades on HF paths would give. So it is reasonable to assume a small tone-to tone amplitude variation will have no noticeable effect on decoding efficiency.

To completely avoid the spectral hole at 0Hz caused by the coupling capacitors, DC coupling of the D/A to the upconverter would be ideal. A 0-5V output from the D/A can be converted to 0.7 - 1.7V

by using three resistors and use of the 5V rail as a biassing offset. The calculation of these resistor values for any arbitrary input and output range is a seemingly simple task that is anything but.

It has been demonstrated with this first generation hardware used for the GB3SCS beacon that it is possible to generate a modulating waveform in a custom low frequency DDS implemented on a PIC. This is controlled over a similar SPI interface to that used for many other frequency sources. Suitable level shifting allows the waveform to drive a single chip quadrature upconverter to RF. Using this technique allows an RF source to be optimised for phase noise and spurii at single frequency.

References

[1] http://www.g4jnt.com/SCRBG/ The Bell Hill Beacons

[2] https://www.youtube.com/watch?v=bnrLfm00Wys Reverse DDS Explained by G4NNS

[3] http://www.g4jnt.com/SCRBG/TheNewGB3SCS.htm The old GB3SCS beacon design

[4] RadCom, February 2012, Design Notes, *Integrated quadrature up- and downconverters.*

[5] http://g4jnt.com/ADL5375_Tests.pdf Using the ADL5375 I/Q upconverter

[6] https://g4jnt.com/adf4150-ctl2.zip Control of ADF4xxx synthesizers